ABSTRACT

A selectively enabled clamp circuit for limiting voltage overshoot on an input/output (I/O) pin of an associated integrated circuit (IC) device includes a single discharge transistor and a select circuit. The single discharge transistor is connected between the I/O pin and ground potential, and the select circuit is coupled to the I/O pin and includes an input to receive an enable signal and an output coupled to a gate of the signal discharge transistor. For some embodiments, the select circuit includes a level shifter circuit and a voltage detection circuit.